terminal to a logic standard selected from the group consisting of TTL, CMOS, GTL and HSTL.

75. (Amended) The method of claim 74, wherein the modifying further comprises modifying the input signal to comply with a logic standard selected from the group [including:] consisting of TTL, CMOS, open drain logic, GTL, terminated HSTL, and non-terminated HSTL.

REMARKS

I. Introduction

Claims 35-75 are pending in the application.

Applicants note with appreciation that the Examiner has allowed claims 35-51 and has indicated that claims 53, 56 and 63 contain subject matter allowable over the prior art.

Claims 53, 56, and 63 are objected to as being dependent on a rejected base claim.

Claims 52, 54-55, 57-62 and 64-75 are rejected under 35 U.S.C. § 102(e).

Reconsideration of this application in light of the following remarks is respectfully requested.

II. Information Disclosure Statement

As suggested, applicants include herewith an Information Disclosure Statement and corresponding PTO-1449 form listing the prior art cited against the parent case (U.S. Patent 5,970,255). Also included are copies of the cited references.

III. Compliance with 37 C.F.R. 1.178

Assignee acknowledges the requirement under 37 C.F.R. 1.178 that surrender of the original patent (U.S. Patent 5,970,255) is required before this application can be allowed. Assignee will determine whether to surrender the original patent after the case has been decided on the merits.

Moreover, assignee hereby informs the Examiner that U.S. Patent 5,970,255 was involved in ITC Proceeding 337-TA-453 between Altera (assignee) and Xilinx Corporation. The ITC proceeding was settled by joint motion on October 17, 2001.

IV. Claim Objections

Claims 35-75 are objected to for failure to submit a separate paper setting forth the status of all claims and an explanation of the support in the disclosure of the patent for the changes made to the claims. Applicants submit herewith a

claim chart showing support for the features recited in claims 35-75.

Claims 38 and 62-63 are objected to for minor informalities. In particular, applicants have amended claim 62 to remove the recitation of "an input buffer" in order to cure an alleged antecedent basis problem. Minor misspellings have been corrected in the amendments to claims 38 and 67.

Claims 37, 38, 50, 53-55, 63-65, 72 and 75 are objected to as allegedly not being in proper Markush form. Applicants have amended those claims as suggested by the Examiner.

Claims 52, 56, 59, 62, 68, 71 and 74 are objected to for lack of support. Support for the "differential logic standard" feature may be found at column 4, lines 1-13 (GTL and HSTL are differential logic standards) among other places as demonstrated by the claim chart below.

Applicant amends the specification and drawings to correct minor typographical errors. In particular, applicants have changed two instances of a reference designation (from 102 to 104) that were inadvertently mislabeled. Also, applicants have changed transistor 412 in FIG. 4 from a PMOS type to an NMOS type to make it consistent with the

specification. No new matter has been added as a result of these amendments.

Claim	Status	Support*
1-34	Canceled	
35. A programmable input/output device for coupling a programmable logic device (PLD) to external circuitry, the input/output device comprising:	Pending	Column 2, lines 20-49; and FIGS. 1-5
an input/output pad;		Column 3, lines 15 and 26; and FIG. 1, item 106
an output buffer adapted to receive output signals from the PLD, the output buffer modifying the output signals and being coupled to the input/output pad;		Column 3, line 16-20, FIG. 1, item 102
an input buffer adapted to receive a reference signal and input_signals from the input/output pad and from the output buffer, the input buffer comparing the received input signals to the reference signal to produce a differential signal and coupling the differential signal to the PLD to provide the PLD with modified input signals; and		Column 6, lines 36-45 and FIG. 3

* Support for the listed claim features is merely illustrative not meant to be exhaustive. Additional support for these features may be found in other portions of the '255 patent.

a plurality of programmable elements that select the standard with which the output buffer and the input buffer respectively modify the output and input signals.		Column 3, lines 47-57; and FIG. 1, items 108 and 110
36. The programmable input/output device of claim 35, wherein the plurality of programmable elements further comprise: a first programmable element coupled to the output buffer and the input buffer; and	Pending	Column 3, lines 47-57; and FIG. 1, item 108
a second programmable element coupled to the output buffer.		Column 3, lines 47-57; and FIG. 1, item 110
37. The programmable input/output device of claim 36, wherein the plurality of programmable elements are elements selected from the group consisting of SRAM, EPROM, EEPROM, fuse and antifuse elements.	Pending	Column 3, lines 30-35
38. The programmable input/output device of claim 35, wherein the input/output device provides signal modification in accordance with logic standards from the group consisting of TTL, CMOS, GTL, and HSTL.	Pending	Column 3, lines 65-67 to Column 4, line 9 (Table 1)
39. The programmable input/output device of claim 35, wherein the input buffer comprises: a differential amplifier circuit being adapted to receive the input signals;	Pending	Column 6, lines 36-45 and FIG. 3

control circuitry that controls the modification of the input signals in accordance with the standard selected by the plurality of programmable elements; and		Column 3, lines 65-67 to Column 4, line 9 (Table 1)
inversion circuitry that provides the modified input signals to the PLD.		Column 7, lines 5-13; and FIG. 3, items 314, 316, and 318
40. The programmable input/output device of claim 39, wherein the differential amplifier circuit and the control circuit operate in conjunction with each other to provide the modifications of the input signals in accordance with a plurality of logic standards.	Pending	Column 5, line 66 to column 6 line 45; FIG. 3
41. The programmable input/output device of claim 39, wherein the differential amplifier circuit and the input buffer operate independent of each other such that the modifications of the input signals are performed by the input buffer in accordance with a first logic standard and by the differential amplifier circuit in accordance with a second logic standard, the first and second logic standards being selected by the plurality of programmable elements.	Pending	Column 7, line 48 to 54; FIG. 4

42. The programmable input/output device of claim 41, wherein the input buffer is optimized for speed to provide modification in accordance with the first logic standard at increased speed.	Pending	Column 7, lines 48-54; FIG. 4
43. The programmable input/output device of claim 41, wherein the differential amplifier circuit is optimized for speed to provide modification in accordance with the second logic standard at increased speed.	Pending	Column 7, lines 48-54; FIG. 4
44. A programmable input/output device for coupling a programmable logic device (PLD) to external circuitry, the input/output device comprising:	Pending	Column 2, lines 20-49; and FIGS. 1-5
means for receiving output signals from the PLD and for modifying the output signals in accordance with a selected logic standard, the means for receiving providing the modified output signals to the means for coupling;		Column 2, lines 20-49; and FIGS. 1-5

means for coupling the input/output device to the external circuitry; means for modifying input signals received from the means for receiving and the means for coupling in accordance with the selected logic standard, the means for modifying including a means for comparing the received input signals to a reference signal to produce a differential signal and for providing the modified input signals to the PLD; and		Column 5, line 66 to column 6 line 45; FIG. 3
means for selecting the selected logic standard from a plurality of logic standards.		Column 3, lines 47-57; and FIG. 1, items 108 and 110
45. The programmable input/output device of claim 44, wherein the means for receiving comprises: circuitry for modifying the output signals to an appropriate high voltage level in accordance with the selected logic standard if the output signals are logic high signals; and	Pending	Column 3, lines 47-52, FIG. 1
circuitry for modifying the output signals to an appropriate low voltage level in accordance with the selected logic standard if the output signals are logic low signals.		Column 3, lines 47-52, FIG. 1

46. The programmable input/output device of claim 44, wherein the means for modifying comprises: a first conversion circuit for converting the input signals in accordance with a first logic standard; and	Pending	Column 3, line 48-52; FIG. 1
a second conversion circuit for converting the input signals in accordance with a second logic standard.		Column 3, line 48-52; FIG. 1
47. The programmable input/output device of claim 46, wherein the first and second conversion circuits are merged into a single conversion circuit.	Pending	Column 5, line 66 to column 6 line 2; FIG. 3
48. The programmable input/output device of claim 46, wherein the first and second conversion circuits are substantially independent of each other such that they may be independently optimized for operational speed improvements.	Pending	Column 7, line 28-54; FIG. 4
49. A method for providing a programmable logic device (PLD) with the capability of being selectively coupled to external circuitry that operates in accordance with a selected one of a plurality of logic standards, the method comprising: programmably selecting the selected one of a plurality of logic standards;	Pending	Column 2, lines 31-43

modifying output signals from the PLD in accordance with the selected logic standard such that high PLD signals correspond to high signals of the selected standard and low PLD signals correspond to low signal of the selected standard;		Column 3, lines 17-24
receiving input signals from an external interface;		Column 3, lines 25-26
comparing the received input signals to a reference signal to produce a differential signal in accordance with the selected logic standard such that high input signals are converted to high PLD signals and low input signals are converted to low PLD signals.		Column 3, lines 25-28, column 6, lines 37-45
50. The method of claim 49, wherein the programmably selecting further comprises selecting a logic standard from the group consisting of TTL, CMOS, open drain logic, GTL, terminated HSTL, and non-terminated HSTL.	Pending	Column 3, line 65 to column 4, line 13
51. The method of claim 49, wherein the programmably selecting further comprises applying a plurality of Select Bits to a plurality of programmable elements.	Pending	Column 3, lines 22-24
52. A programmable input/output device capable of operating at multiple logic standards comprising: an input/output terminal;	Pending	Column 2, lines 31-43

a plurality of programmable elements; and		Column 3, lines 15-18
an input buffer having circuitry controlled by at least one of the plurality of programmable elements to select between a first logic standard and a second logic standard wherein the second logic standard is a differential logic standard.		Column 3, lines 15-18; column 4, lines 1-13 (GTL and HSTL are differential logic standards)
53. The programmable input/output device of claim 52 wherein the differential logic standard is a standard selected from the group consisting of HSTL and GTL.	Pending	Column 4, lines 1-153
54. The programmable input/output device of claim 52 wherein the first logic standard is a standard selected from the group consisting of TTL or CMOS.	Pending	Column 4, lines 1-13
55. The programmable input/output device of claim 52 wherein the programmable elements are elements selected from the group consisting of SRAM, EPROM, EEPROM, and antifuse elements.	Pending	Column 3, lines 30-35
56. The programmable input/output device of claim 52 wherein the input buffer further comprises a differential amplifier circuit that is used for generating the differential logic standard.	Pending	Column 6, lines 36-45

57. The programmable input/output device of claim 52 wherein at least one programmable element is coupled to the input buffer.	Pending	Column 3, lines 29-30
58. The programmable input/output device of claim 52 further comprising an output buffer having circuitry controlled by at least one of the plurality of programmable elements to select between the first logic standard and the second logic standard.	Pending	Column 3, lines 16-24; column 4, lines 1-13
59. The programmable input/output device of claim 58 wherein the second logic standard is a differential logic standard.	Pending	column 4, lines 1-13 (GTL and HSTL are differential logic standards)
60. The programmable input/output device of claim 58 wherein at least one programmable element is coupled to the input buffer.	Pending	Column 3, lines 29-30
61. The programmable input/output device of claim 60 wherein the input buffer and the output buffer are controlled by the same programmable element.	Pending	Column 3, lines 21-30; and FIG. 1, item 108
62. A programmable input/output buffer capable of operating at multiple logic standards comprising: an input/output terminal;	Pending	Column 2, lines 12-24; FIG. 1
a plurality of programmable elements;		Column 2, lines 12-24; FIG. 1

an output buffer having circuitry controlled by at least one of the plurality of programmable elements to select between one logic standard and a differential logic standard.		Column 3, lines 12-24 and line 65 to column 4, line 9; FIG. 1 (GTL and HSTL are differential logic standards)
63. The programmable input/output device of claim 62 wherein the differential logic standard is a standard selected from the group consisting of HSTL and GTL.	Pending	Column 4, lines 1-15
64. The programmable input/output device of claim 62 wherein the first logic standard is a standard from the group of TTL and CMOS.	Pending	Column 4, lines 1-15
65. The programmable input/output device of claim 62 wherein the programmable elements are elements selected from the group consisting of SRAM, EPROM, EEPROM, and antifuse elements.	Pending	Column 3, lines 32-35
66. The programmable input/output device of claim 62 wherein at least one programmable element is coupled to the output buffer.	Pending	Column 3, lines 22-24; FIG. 1, items 108 and 110
67. The programmable input/output device of claim 62 further comprising an input buffer having circuitry controlled by at least one of the plurality of programmable elements to select between the first logic standard and the second logic standard.	Pending	Column 3, lines 25-35 and column 4, lines 1-13

68. The programmable input/output device of claim 67 wherein the second logic standard is a differential logic standard.	Pending	Column 4, lines 1-13 (GTL and HSTL are differential logic standards)
69. The programmable input/output device of claim 67 wherein at least one programmable element is coupled to the output buffer.	Pending	Column 3, lines 22-24 and FIG. 1, item 110
70. The programmable input/output device of claim 69 wherein the input buffer and the output buffer are controlled by the same programmable element.	Pending	Column 1, lines 12-24; FIG. 1, item 108
71. A programmable input/output device comprising: an input/output terminal;	Pending	Column 3, lines 12-24
an input buffer and an output buffer coupled to the input/output terminal, each of which includes means for modifying signals applied to the input/output terminal to a selected one of multiple logic standards wherein at least one of the multiple logic standards is a differential logic standard; and		Column 3, lines 12-24; column 4, lines 1-13
a plurality of programmable elements for selecting the logic standard at which the input and output buffers operate.		Column 3, lines 47-58

72. The programmable input/output device of claim 71 wherein the input buffer and the output buffer further comprise means for modifying signals applied to the input/output terminal to a logic standard selected from the group consisting of TTL, CMOS, GTL and HSTL.	Pending	Column 3, lines 12-24 and column 4, lines 1-13
73. The input/output device of claim 71, wherein the input buffer and the output buffer share at least one programmable element.	Pending	Column 3, lines 12-24 and FIG. 1, item 108
74. A method of operating a programmable input/output device at a selected one of multiple logic standards, the method comprising: selecting a logic standard;	Pending	Column 3, lines 12-24
receiving an input signal at an input of the input/output device; and		Column 3, lines 12-24
modifying the input signal based on the selected logic standard; wherein at least one of the multiple logic standards is a differential logic standard.		Column 3, lines 12-24; column 4, lines 1-13 (GTL and HTSL are differential logic standards)
75. The method of claim 74, wherein the modifying further comprises modifying the input signal to comply with a logic standard selected from the group consisting of TTL, CMOS, open drain logic, GTL, terminated HSTL, and non-terminated HSTL.	Pending	Column 3, lines 12-24; column 4, lines 1-13 (GTL and HTSL are differential logic standards)

V. The Rejections Based on 35 U.S.C. § 102(e)

The Examiner rejected claims 52, 54-55, 57-62 and 64-75 under 35 U.S.C. § 102(e), as being anticipated by Pierce et al. U.S. Patent 5,581,199 (hereinafter "Pierce"). Applicants respectfully traverse.

The Examiner rejected the above-identified claims contending that Pierce teaches applicants' invention substantially as claimed, including a plurality of programmable logic elements to select between a first logic standard and a second logic standard wherein the second logic standard is a differential logic standard. Applicants respectfully disagree.

Claims 52, 62, 71 and 74 and are directed towards methods and apparatus that allow an electronic device to select a logic standard from at least one of two available logic standards (one being differential) and operate at the selected standard. One advantage of this configuration is that it provides an I/O architecture that can easily adapt to external environments that operate different logic levels. One deficiency of prior art electronic devices is that their I/O circuitry is typically compatible with only one type of logic standard. Thus, if an end user needs to connect to external circuitry employing standard TTL logic (Transistor-

to-Transistor Logic), an electronic device that can provide and receive the appropriate drive signals is needed. However, simply changing the external environment to one that operates at a different logic standard, such as an open-drain CMOS, may require a different electronic device, although the basic device is substantially the same. Applicants' invention solves this problem by providing I/O devices and methods that allow the user to programmably select any one of several logic standards, so that a single electronic device is adaptable and may be used with external circuitry that operates at different logic levels.

In contrast, Pierce fails to show or suggest this feature anywhere. The Examiner has suggested that Pierce shows circuitry capable of operating at first and second logic standards in FIG. 16 and at column 19, lines 14-65 (Office Action at page 4). This is simply not the case. Register 181 is merely an RS flip-flop that acts as a latch. It is well known in the art that flip-flops are only capable of operating at a single logic standard (although Q and QL represent that the output may change between a logic high and a logic low level within that one logic standard). Logic gates 178 and 180 merely feed the set and reset inputs of RS flip-flop 181. Nowhere in Pierce are I/O circuits shown that can switch

between multiple logic standards as described in applicants' claims. Accordingly, claims 52, 62, 71 and 74 and those that depend therefrom are allowable.

VI. The Drawings

Applicant respectfully requests approval for the following amendment to FIG. 4 that is indicated in red ink on the attached photocopy of FIG. 6. The proposed amendment merely changes transistor 412 from a PMOS type to an NMOS type as described in the specification. No new matter would be added as a result of this proposed amendment. Moreover, in compliance with 37 C.F.R § 1.173(b)(3), applicants also provide a formal drawing copy of amended FIG. 3 for inclusion with any Reissue Patent that may result from this case.

VII. Conclusion

The foregoing demonstrates that claims 52-75 are allowable. Accordingly, this application is in condition for allowance.

Reconsideration and allowance are therefore respectfully requested.

Respectfully submitted,

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